REMARKS

In the Office Action mailed June 28, 2004, claims 1-27 are rejected under 35 USC §102(e) as being anticipated by Haroun et al., (US Patent 6,324,662, hereinafter "Haroun").

In response to the rejection, Applicant has amended independent claims 7, 14 and 21 to overcome the rejection. Applicant has also amended claims 8 and 25 to conform the claims to the amended independent claims 7 and 21, respectively. Applicant respectfully requests reconsideration of the remaining claims.

In response to the rejection of claims 1-6, Applicant respectfully submits that Haroun fails to disclose or suggest the method for flexibly nesting JTAG TAP controllers. In particular, independent claim 1 recites a method for flexibly nesting JTAG TAP controllers for IP cores comprising steps of:

> (i) selecting at least one available bit from a selectable bit register; and
>
> (ii) extending an apparent length of an instruction register of said host JTAG TAP controller by using said at least one available bit from said selectable bit register.

That is, Haroun fails to disclose or suggest "a selectable bit register," or extending the apparent length of an instruction register by a bit from the selectable bit register. It is suggested in the Office Action that link shift register 406 of Haroun comprises a "selectable bit register," and that the selection of the available bit data signal 460 extends an apparent length of an augmentation shift register (AISR) 410. However, a selectable bit register as claimed by Applicant enables the selection of various register sizes, for example in response to a size selection signal. There is no disclosure or suggestion that link shift register 406 comprises a selectable

bit register, or that an apparent length of an instruction register is extended by the bits selected from the link shift register 406. That is, there is no suggestion that anything other than all of the bits are output by the link shift register 406.

Further, Haroun teaches away from Applicant's invention by teaching supplementing data which is output by a register with a fixed number of bits. That is, Haroun discloses an augment instruction register 410 which always receives two additional bits (used for instruction scan operations). In particular, Haroun requires that the two bits shifted into the AISR 410 during the 1149.1 instruction scan operation must provide at least two codes, a TAP scan code and a TLM scan code. That is, output multiplexer 414 of Haroun either outputs the selected bits of one of TD01 through TD05, or the selected bits of one of TD01 through TD05 shifted by a fixed two bit input 454 (Col. 7, line 61 - Col. 8, line 4). Accordingly, Haroun does not disclose or suggest extending the apparent length of an instruction register by using bits from a selectable bit register. Applicant submits that claims 2-6, which are dependent upon claim 1, are allowable for the same reason that claim 1 is believed allowable.

In response to the rejection of independent claim 7, Applicant has amended the claim to include a step of "selecting an apparent register size based upon a number of IP cores implemented in the FPGA-based SoC." Applicant respectfully submits that Haroun fails to disclose or suggest enabling selecting an apparent register size. Haroun merely discloses coupling a fixed number of bits (i.e. two bits) comprising a TAP scan code and a TLM scan code to a register in order to enable instructions scan operations, as described above. Applicant has amended claim 8 to conform the claim to the amended claim 7. Applicant submits that dependent claims 8-10 are allowable for the same reasons that independent claim 11 is believed allowable.

In response to the rejection of claim 11, Applicant respectfully submits that independent claim 11 is believed allowable for the same reason that independent claim 1 is believed allowable. That is, for the same reasons set forth above with respect to claim 1, Haroun fails to disclose or suggest a selectable bit register or a selector for extending the apparent length of an instruction register by a bit from the selectable bit register. Applicant submits that dependent claims 12 and 13 are allowable for the same reasons that independent claim 11 is believed allowable.

In response to the rejection of independent claim 14, Applicant has amended the claim to recite:

> "an instruction register size select signal enabling the selection of an apparent register size to accommodate a variable number of IP cores."

Applicant respectfully submits that Haroun fails to disclose or suggest a signal for enabling the selection of an apparent register size, and in particular the selection of an apparent register size to accommodate a variable number of IP cores. Applicant submits that dependent claims 12 and 13 are allowable for the same reasons that independent claim 11 is believed allowable.

In response to the rejection of claim 18, Applicant respectfully submits that Haroun fails to disclose the method as claimed. Claim 18 is a method claim directed to ensuring that an information register length for nested JTAG TAP controllers for IP cores remain the same before and after configuration of an FPGA in an FPGA-based system-on-chip (SoC). In particular, the method of claim 18 comprises steps of:

> "forming connections between FPGA JTAG logic of the FPGA and IP Core JTAG logic of the IP core using a programmable interconnect; and
>
> emulating an instruction register of the IP core prior to configuration of the FPGA using a shift register of the same length as the instruction register of the IP core."

Applicant respectfully submits that Haroun fails to disclose or suggest the use of a field programmable gate array (FPGA) in a SoC, and therefore could not disclose forming connections between FPGA JTAG logic of the FPGA and IP Core JTAG logic of the IP core using a programmable interconnect, as claimed by Applicant. Similarly, because Haroun does not disclose an FPGA, Haroun could not disclose emulating an instruction register of the IP core prior to configuration of the FPGA. Haroun also could not disclose the configuration of the FPGA using a shift register of the same length as the instruction register of the IP core. Applicant submits that dependent claims 19 and 20 are allowable for the same reason that independent claim 18 is believed allowable.

Finally, in response to the rejection of claim 21, Applicant has amended claim 21 to indicate that the host JTAG TAP controller comprises "a selectable bit register enabling the selection of an apparent register size to accommodate a variable number of IP cores." As set forth above, Haroun fails to disclose or suggest a selectable bit register enabling the selection of an apparent register size, and in particular selecting an apparent register size to accommodate a variable number of IP cores. Applicant has amended dependent claim 25 to properly claim the selectable bit register, which now has antecedent basis in claim 21. Applicant submits that dependent claims 22-27 are allowable for the same reasons that independent claim 21 is believed allowable.

CONCLUSION

All claims are in condition for allowance and a Notice of Allowance is respectfully requested. If there are any questions, the Applicant's attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on September 27, 2004.

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Signature